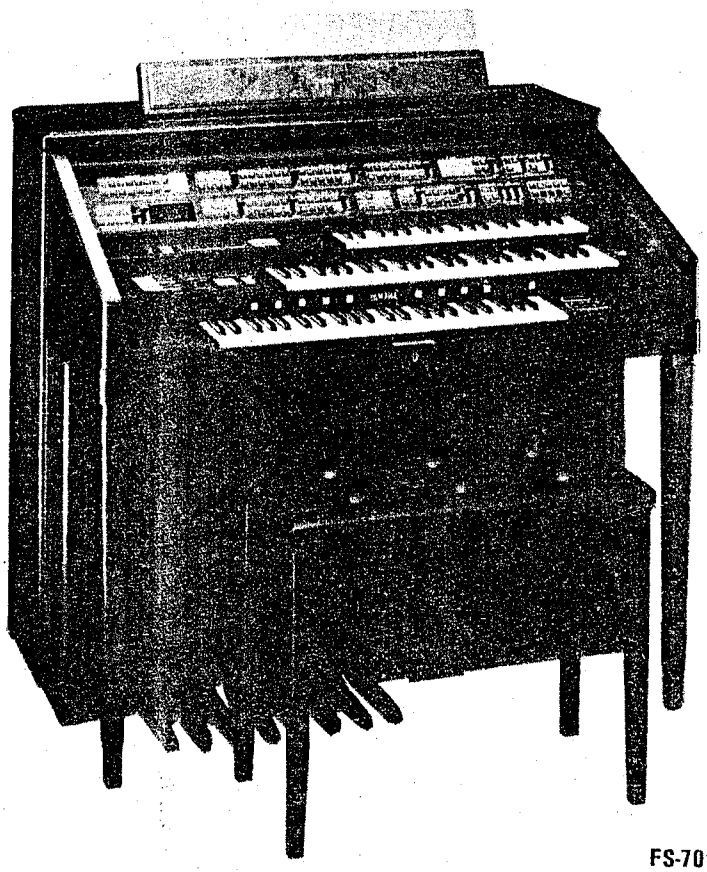
YAMAHA ELECTONE®

FS-70/FS-50

SERVICE MANUAL



FS-70

001169

SINCE 1887 YAMAHA
NIPPON GAKKI CO., LTD. HAMAMATSU, JAPAN
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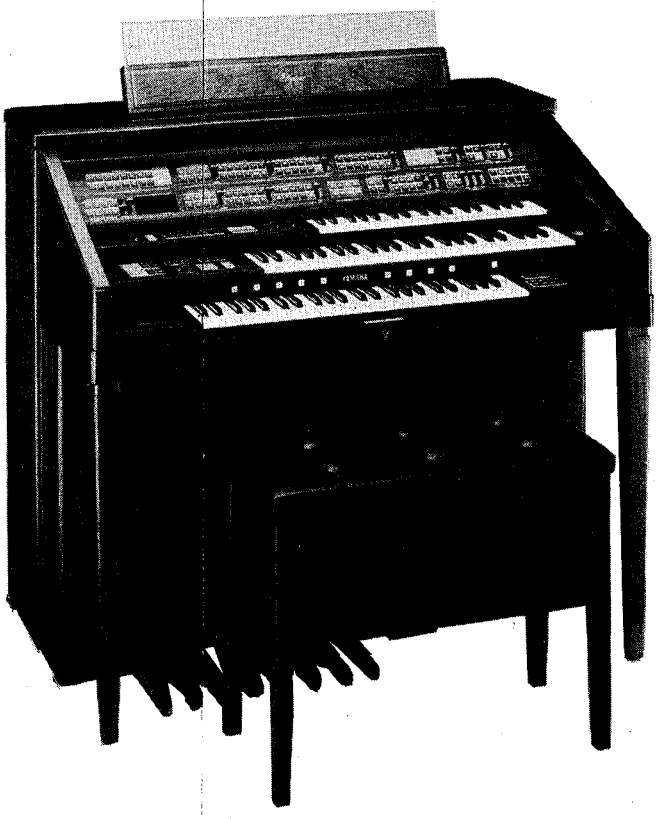
CONTENTS (目次)

FS-500, 300	: Model names only for U.S.A. アメリカでの機種名です。
FS-70, 50	: Model names except for U.S.A. アメリカ以外での機種名です。

FS-70



FS-50

SPECIFICATIONS

Italics: FS-70

KEYBOARDS
- *Solo:* *37 keys c_1 ~ c_4 (3 octaves)*
- Upper: 49 keys c ~ c_4 (4 octaves)
- Lower: 49 keys C ~ c_3 (4 octaves)
- Pedals: 13 keys C ~ c (1 octave)

COMBINATION
- Upper: Combi. Lever, Memory 1 · 2 · 3, Preset 1 · 2 · 3 · 4, Volume, (Levers) 16′, 8′, 5⅓′, 4′, 2⅔′, 2′, 1′, Attack 4′ · 2⅔′ · 2′, Attack Length
- Lower: Combi. Lever, Memory 1 · 2 · 3, Preset 1 · 2 · 3 · 4, Volume, (Levers) 8′, 4′, 2⅔′, 2′
- Pedals: Combi. Lever, Memory, Preset 1 · 2, Volume, (Levers) 16′, 8′

ORCHESTRA
- Upper: Strings 1, Strings 2, Strings 3, Brass 1, Brass 2, Reed 1, Reed 2, Vocal, Spice 1, Spice 2, (Controls) Preset Vibrato, Touch Tone, Volume
- Lower: Strings 1, Strings 2, Brass 1, Brass 2, Reed, Vocal, Spice 1, Spice 2, (Controls) Preset Vibrato, Touch Tone, Volume

SPECIAL PRESETS
- Upper: Piano, Harpsichord, Celesta, Vibraphone, Marimba, Mandlin, Banjo, Jazz Guitar, Brass 1, Brass 2, Cosmic, (Controls) Touch Tone, Volume
- Lower: Piano, Electric Piano, Harpsichord, Harp, Acoustic Guitar, Jazz Guitar, Brass 1, Brass 2, Cosmic, (Controls) Touch Tone, Volume

CUSTOM VOICES
- Upper/Lower: Flute, Oboe, Clarinet, Saxophone, Trumpet, Trombone, Violin, Jazz Guitar, Cosmic 1, Cosmic 2, Cosmic 3, (Controls) Preset Vibrato, Touch Vibrato, Touch Tone, Volume
- Pedals: Contra Bass 1, Contra Bass 2, Contra Bass 3, Tuba, Electric Bass 1, Electric Bass 2, Electric Bass 3, Vocal, (Controls) Brilliance, Volume

SOLO

Piccolo, Flute, Oboe, Clarinet, Saxophone, Trumpet 1, Trumpet 2, Horn, Trombone, Voilin, Jazz Guitar, Harmonica, Cosmic 1, Cosmic 2, (Controls) Detune, Coupler, Transposition (Down, Normal, Up), Preset Vibrato, Touch Vibrato, Touch Tone, Brilliance, Volume, Slide Control

ENSEMBLE

Upper Combi., Upper Orches., Upper Special, Upper Custom, Lower Combi., Lower Orches., Lower Special, Lower Custom

EFFECTS · CONTROLS
- Sustain: (Switches) Upper Sustain (Knee), Lower Sustain (Knee), Pedal Sustain, (Controls) Upper, Lower, Pedal,
- Symphonic: Celeste, Symphonic, Upper Combi., Upper Orches., Lower Combi., Lower Orches.,
- Tremolo: Chorus, Tremolo, Upper Combi., Upper Orches., Lower Combi., Lower Orches., Tremolo Speed control,
- Reverb, Glide (Foot Switch control),
- (Combination) Program Set, Response Fast, Timbre Variation,
- Vibrato Presetter: Set, Lever, Player, Preset, (Controls) Touch Depth, Delay, Depth, Speed, (Indicator) *Solo*, Upper Orches., U/L Custom, Lower Orches., Pedals

AUTO RHYTHM
- Pattern Selectors: March, Waltz, Ballad, Swing, Bounce, Slow Rock, 8 Beat 1, 8 Beat 2, Tango, Latin 1, Latin 2, Bossanova, Samba, Latin Rock, Disco, 16 Beat, Variation 1 · 2 · 3 · 4,
- Break Variation: 1 · 2 · 3 (16x3 patterns), Break, Break Variation (Foot Switch control)
- Auto Variation: Normal, 4Bar, 8Bar, 16Bar,
- Rhythm Sequence Programmer: Program 1 · 2 · 3 · 4 (64Bars x 4), On, Record, Blank, End, Back, Forward,
- Digital Display: Tempo, Bar/Beat,
- Controls: Synchro Start, Start, Tempo, Volume, Balance, Tempo Indicator Lamp, Rhythm Stop (Foot Switch control)

AUTO ARPEGGIO
- Pattern Selectors: 1 · 2 · 3 · 4 · 5 · 6 · 7 · 8 (16x8 patterns),
- Voice Selectors: Piano, Harpsichord, Strings, Harp, Volume (control)

RHYTHMIC CHORD
- Pattern 1: Piano, Jazz Guitar, Solid Guitar, Phaser (effect), Volume (control),
- Pattern 2: Brass, Jazz Guitar, Solid Guitar, Phaser (effect), Volume (control),

AUTO BASS/CHORD
- Mode Selectors: Normal, Single Finger Chord, Fingered Chord, Custom A.B.C.,
- Multi Bass (Normal, 1, 2, 3), Lower Memory, Pedal Memory

PLAY ASSIST
- Functions: Melody On Chord 1, Melody On Chord 2, Duet, Counter Melody,
- Controls: Key Set (Duet control), Play Assist (Knee Lever control),
- Voice Selectors: Upper Combi., Upper Orches., Upper Special

REGISTRATION MEMORY

Preset buttons: 1 · 2 · 3 · 4 · 5 · 6 · 7 · 8,
Controls: Memory, Cancel, Disable, Slider Drive,
Registration Pack: Read, Confirm, Write,
(Indicator) Memory Ready, Error

MAIN CONTROLS

Manual Balance, Master Volume, Expression Pedal, Panel Light switch, Reset, Knee Lever, Foot Switch, Power Switch, Power Light, Pitch Control

OTHER FITTING

Stereo Headphones jack, Aux. Out Left-Right jacks, Aux. In Left-Right jacks, Exp. In jack, Yamaha Tone Cabinet connectors (13 pins · 13 pins), Leslie Tone Cabinet connector (11 pins), Remote (Headphones), Registration Pack, *Panel Light*, Music Rest, Matching Bench, Roll-Top Fallbaord

ACCESSORY JACKS

Input level which produces maximum power

AUX-IN (Left, Right)	150mVrms
EXP-IN	77.5mVrms
* Input frequency:	1KHz

Input/Output inpedance

AUX-IN (Left, Right)	10KΩ
AUX-OUT (Left, Right)	470Ω
EXP-IN	9KΩ

MAIN AMPLIFIER

Center: 90W(rms), Left: 60W(rms), Right: 60W(rms)

SPEAKERS
- Center: Woofer 30cm (12″), Mid-range 20cm (8″), Tweeter 5cm (2″),
- Left: Mid-range 20cm (8″), Tweeter 5cm (2″),
- Right: Mid-range 20cm (8″), Tweeter 5cm (2″)

CIRCUITRY

Solid State (incl. LSIs and ICs)
Power Consumption: See Electone nameplate
Power Source: 50/60Hz AC

DIMENSIONS
- Cabinet (FS-70): 117(W) x 75(D) x 110(H)cm (46″ x 29½″ x 43½″)
- Cabinet (FS-50): 116(W) x 69(D) x 106(H)cm (45¾″ x 26¼″ x 41½″)
- Bench: 66(W) x 32(D) x 56(H)cm (26″ x 12½″ x 22″)

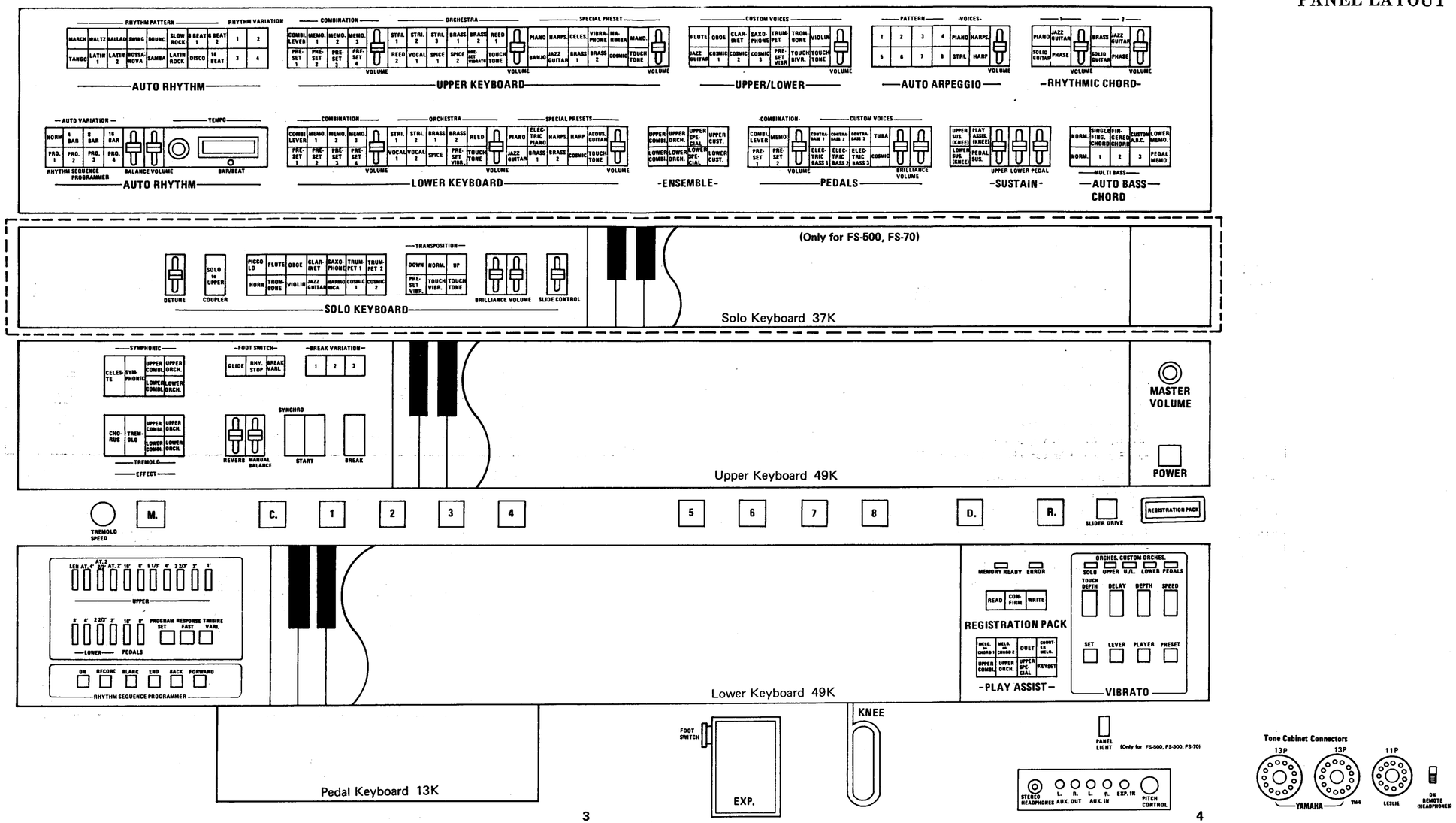
WEIGHTS
- Cabinets (FS-70): 132kg (291 lbs.)
- Cabinets (FS-50): 122kg (269 lbs.)
- Bench: 7.5kg (16.5 lbs.)

FINISH

Real American Walnut

** Specifications subject to change without notice.*

PANEL LAYOUT

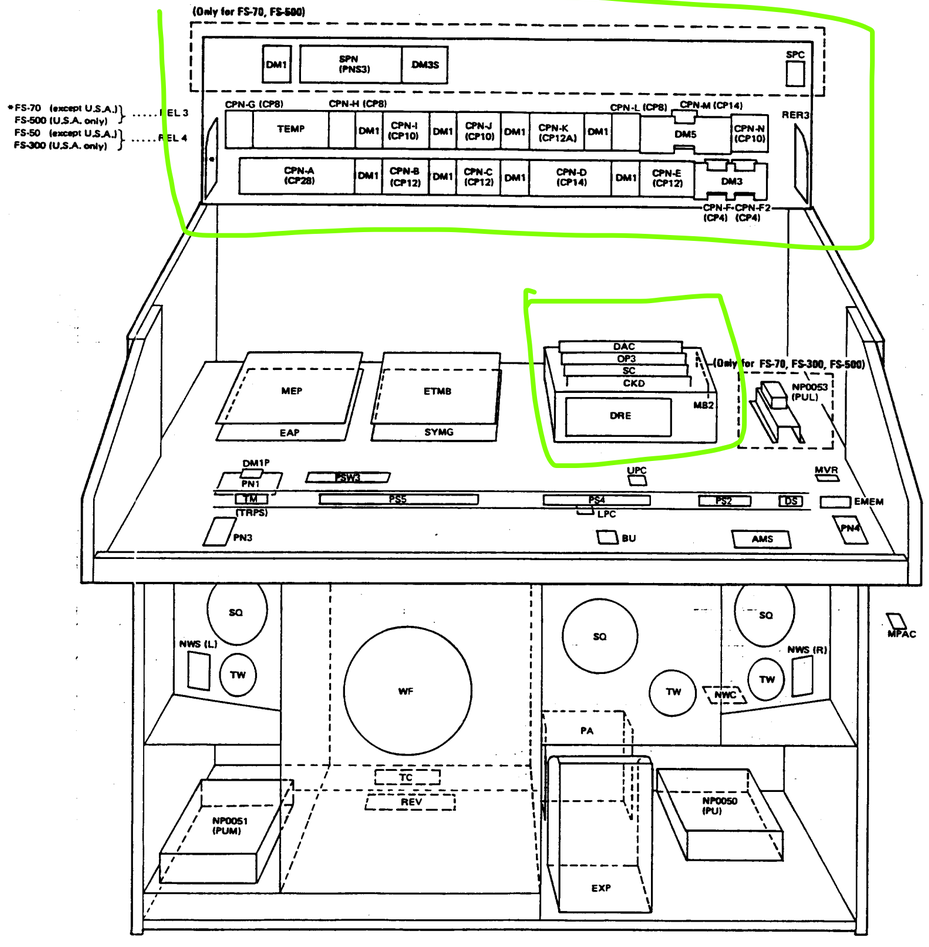


CIRCUIT CONTENTS

CIRCUIT BOARD	FUNCTIONS
CKD	Initial Clear, Two Phase Master Clock OSC (4.8 MHz) System Controller Clock (2.4 MHz) Key Assigner Pitch Control Clock OSC.
SC (System Controller)	System Control Interface System Controller (8 Bit Micro Computer) System Control Decoder System Control Data ROM System Control Data RAM EXT-RAM Interface
OP3	Phase Generator After Touch Envelope Generator Latch Timing Generator Operator-A (Special Presets, Orchestra Family) Operator-B (Combination Family) Operator-E (Custom Voices Family) Operator-RC (Rhythmic Chord I, II) Operator-C (Rhythm) Operator-CW (Rhythm) Rhythm Wave Data ROM
DAC Digital to Analog Converter	Digital Filter-1 Digital Filter-2 Digital Filter-3 Digital to Analog Converter (11 CH. Output) DAC Logic
SPC (only for FS-70, 500) UPC LPC	Solo Key After Touch Sensor Amp. Upper Key After Touch Sensor Amp. Lower Key After Touch Sensor Amp.
MPAC	Registration Pack Module
EXP	Expression Sensor Amp.

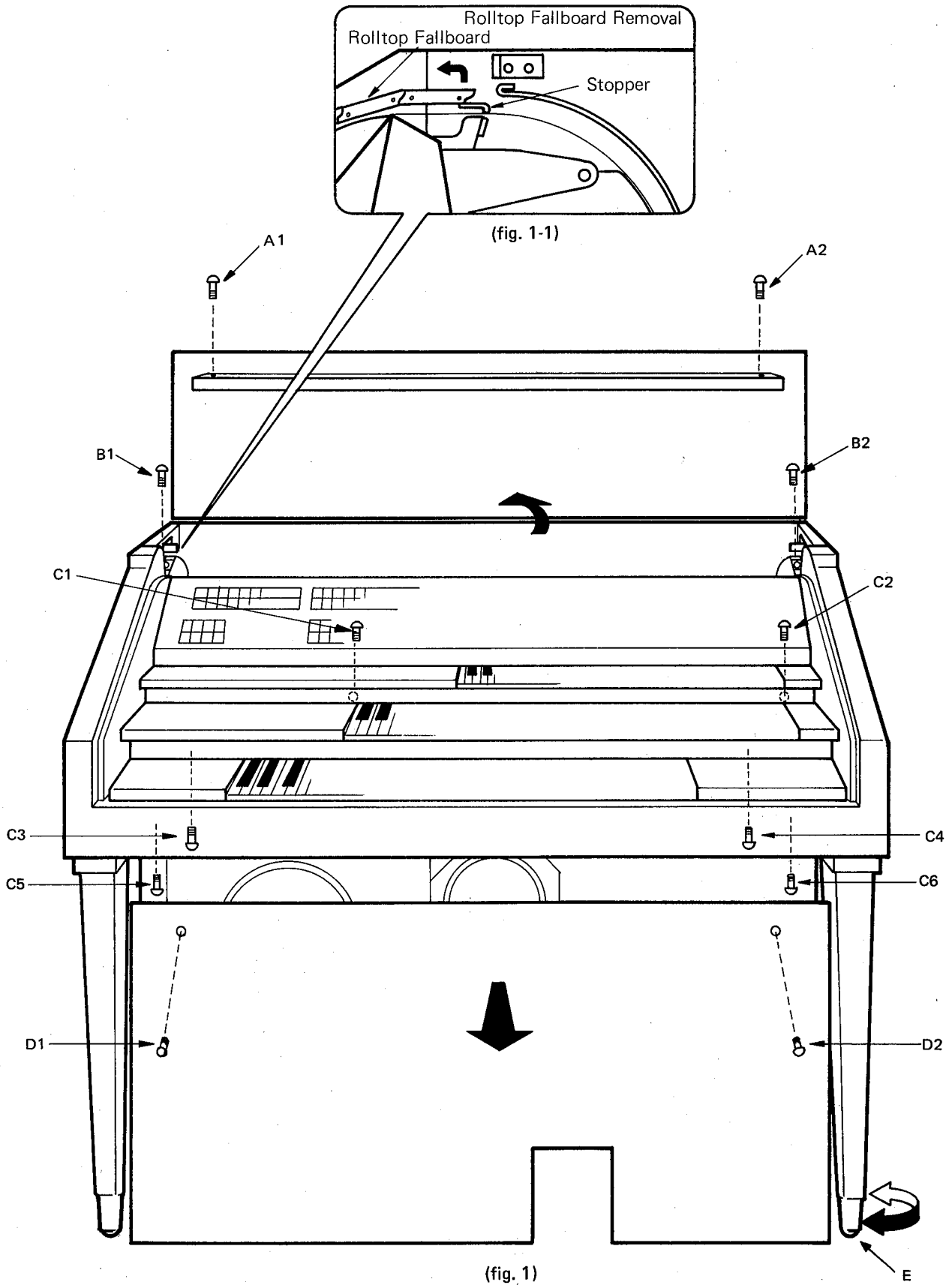
CIRCUIT BOARD	FUNCTIONS
PA	Power Amp. (Center CH. 90W, Right CH. Left CH. 60W)
MEP	Left CH. Center CH. Right CH. Mixing Amps Pre Amps, Photo Couplers (9 CH.) LIN-LOG Converter, V-I Converter Reset Control Gates Reverb Drive Amp. Reverb Pick Up Amp.
EAP	Rhythmic Chord ON/OFF Gates. Phase Shifter Tremolo Clock Generator Tremolo CH. Low Pass Filter (Left, Center, Right) Tremolo Clock Noise Reduction Expander
SYMG	Symphonic Ensemble Clock Generator-I Celeste Gate Control, Compressor, Expander Symphonic Chorus BBD Modulator (3 CH.) (Clock Driver, BBD Modulator, LPF x 2) Symphonic Mixing Amp. (Center, Left, Right)
PUM	±B1V Regulator (Center CH. Power Amp) ±B2V Regulator (Right and Left CH. Power Amp) Muting Control
PU	±12V Regulator, ±15V Regulator +5V Regulator, +12DV Regulator +5M Regulator, Pilot Lamp Power Source (PL, PS)
NWS(L) NWC NWS(R)	Left CH. Dividing Network (2 Way) Center CH. Dividing Network (3 Way) Right CH. Dividing Network (2 Way)
ETMB	Tremolo Tone Filter, Noise Reduction, Compressor Electronic Tremolo BBD Modulator (5 CH.) (Clock Driver, BBD Modulator, AM Modulator x 5) Tremolo CH. Mixing Amp. (Center, Left, Right)

UNIT LAYOUT



- When an unit's name is different from the circuit board's one, the circuit board's name is written in a parenthesis.

DISASSEMBLY PROCEDURE



(fig. 1-1)

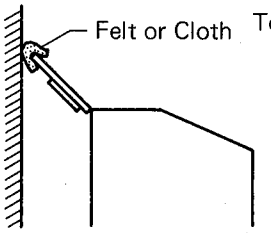
(fig. 1)

Top Board Removal (fig. 1)

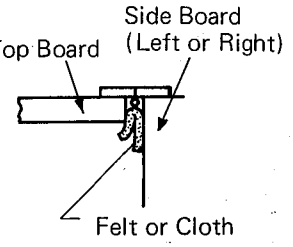
1) Remove the two retaining screws (A1, 2) on the right and left sides.

Note: When the Electone organ is located just in front of wall, cover the top board with cloth to prevent the board to be scratched. (fig. 2)

Note: Lifting up the top board horizontally will scratch the side board. At this time, insert felt or cloth between the top board and side board. (fig. 3)



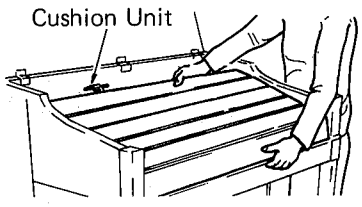
(fig. 2)



(fig. 3)

Rolltop Fallboard Removal

1) Remove two cushion units located at both sides of the rolltop fallboard from the brackets. (fig. 4)
2) Remove the rolltop fallboard by lifting it upward. (fig. 1-1, fig. 4)



(fig. 4)

Control Panel Removal (fig. 1)

1) Remove the screws (B1-2) securing the panel from the both sides.
2) Gently lift up the solo keyboard endblock for the model FS-70, FS-500 (or the shield cover of the control panel reverse side for the model FS-50, FS-300), placing the hands to it.

Keyboard Removal (fig. 1)

Upper Keyboard: Remove the two screws (C1, 2) from the top side, remove the two screws (C3, 4) from the bottom side and then lift up the UK.

Lower Keyboard: Remove the two screws (C5, 6) from the bottom side and lift up the LK.

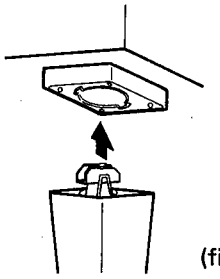
Upper Front Panel Removal

1) Remove the two screws (D1, 2) securing the upper front panel.
2) Insert your hand into the EXP frame from below, lift the front panel upward and remove it towards you.

Front Leg Removal

1) Lift up the front legs off the floor by turning the leg hieght adjusters (fig. 1-E)
2) Turn the front legs to the right or to the left, and remove them.

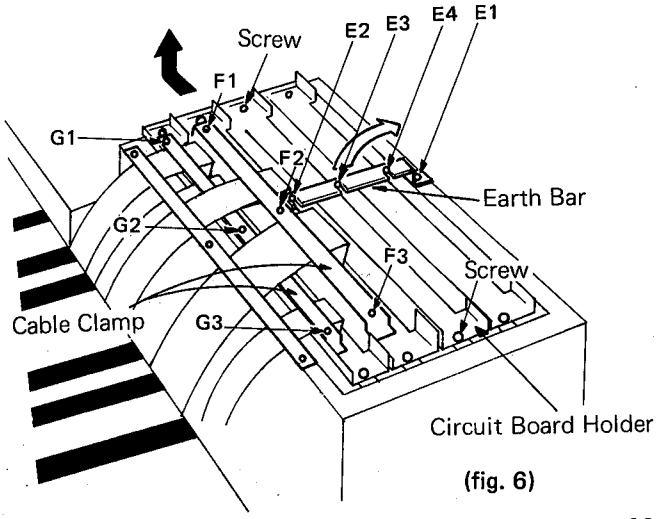
Note on Installation:
1. Put front the leg metal fittings into the leg joint grooves and install the front legs by turning them to the right or to the left. (fig. 5)
2. Adjust each front leg height by turning the leg height adjusters.



(fig. 5)

Digital Circuit Board Removal (fig. 6)

1) Slide the earth bar after loosening the screws (E1-4).
2) Remove the two cable clamps after loosening the screws (F1-3, G1-3).
3) Loosen the two screws securing the circuit board holder.
4) Holding the circuit board holder by hand, slide the circuit board from the MB2 circuit board in the direction indicated by arrow, and lift it up slowly.

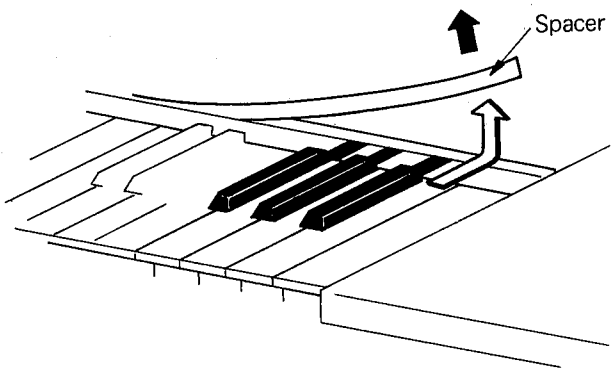


(fig. 6)

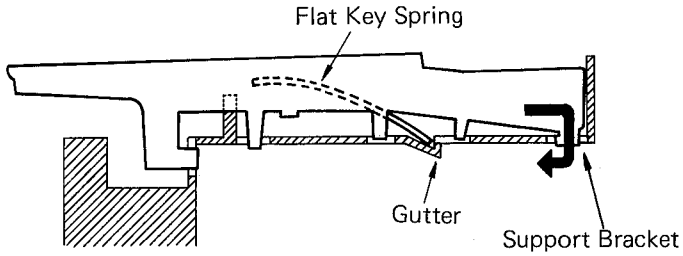
White and Black Key Removal

1) When removing the black keys, remove the white keys beforehand.
2) Remove the spacer. (fig. 7)
3) Pushing the key horizontally, detach it from the support bracket, and lift it up. (fig. 8)

Note on Installation: Align the flat key spring to the gutter, and pushing in the key, inlay it to the support bracket. (fig. 8)

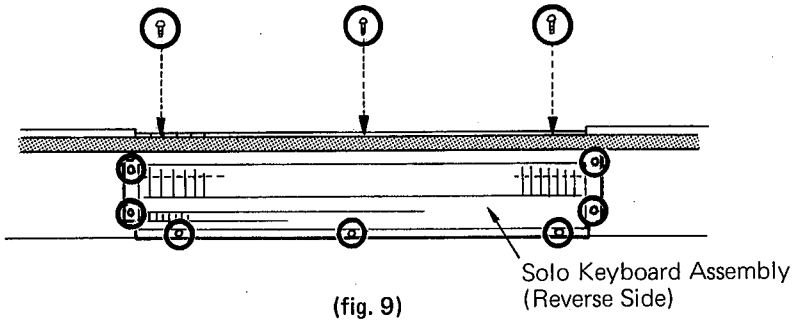


(fig. 7)



(fig. 8)

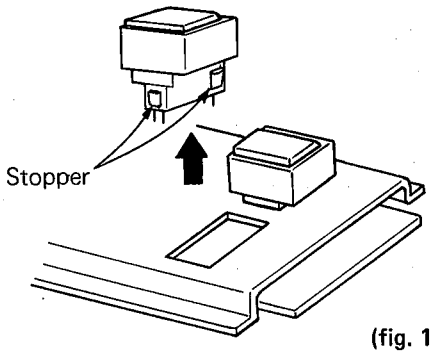
- Solo Key Removal (Only for FS-70, FS-500)
  Remove the ten screws marked with circle and remove the white keys and black keys after removing the solo keyboard assembly.



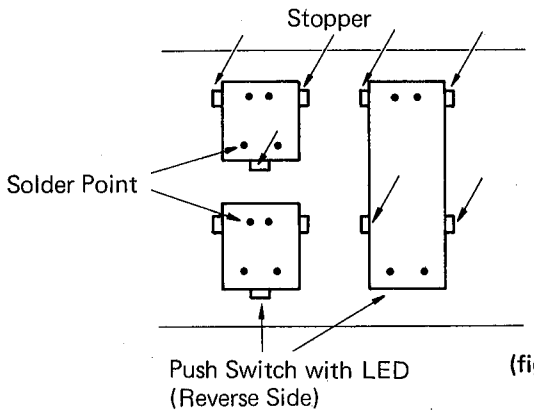
(fig. 9)

Push Switch with LED Removal

1) Remove the panel switch unit (CPN, SPN, PN) form the panel.
2) Take off the solder from the push switch pins (4 soldering points).
3) Remove the push switch by bending the stoppers.



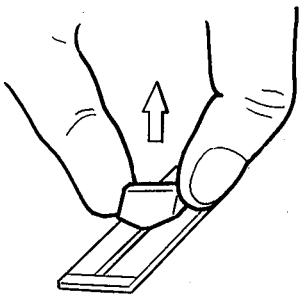
(fig. 10)



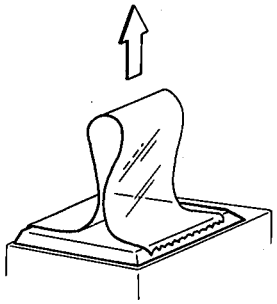
(fig. 11)

Volume Control Knob and Push Switch Button Removal

- Lift up the volume control knob, grasping them with fingers. (fig. 12)
- Remove the buttons from push-button switch by attaching a piece of cellophane tape with fingers and pulling it upwards. (fig. 13)



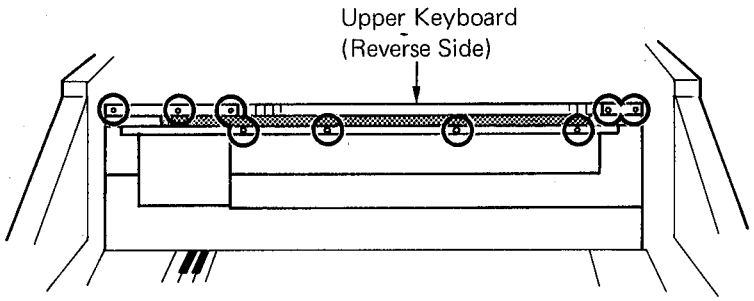
(fig. 12)



(fig. 13)

Registration Memory Button Switch Unit Removal

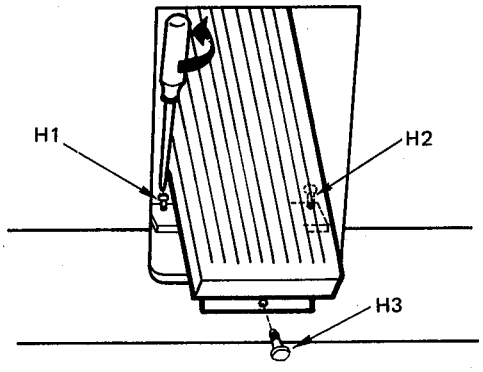
1) Remove the keyboard spacer by removing nine screws marked with circle.
2) Remove each switch unit by removing the retaining screws.



(fig. 14)

Expression Pedal Removal

1) Loosen the two screws (H1, 2).
2) Remove the retaining screw (H3).
3) Remove connector and pull expression pedal out completely.



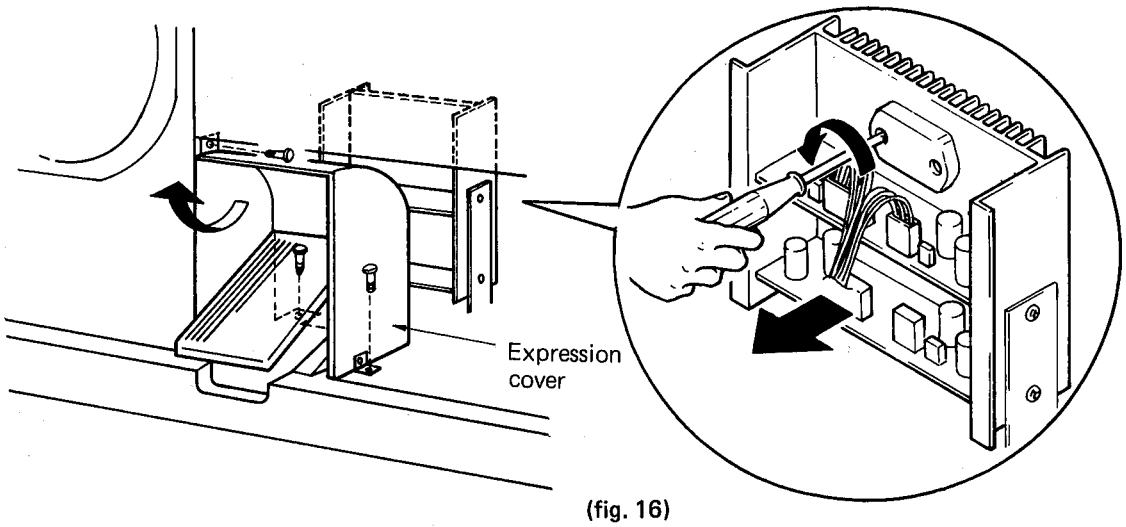
(fig. 15)

Expression Cover Removal

Remove the expression cover by removing the three retaining screws. (fig. 16)

Amplifier Circuit Board Removal

1) Remove the expression cover.
2) Remove the IC retaining screws.
3) Pull out the circuit board towards you.

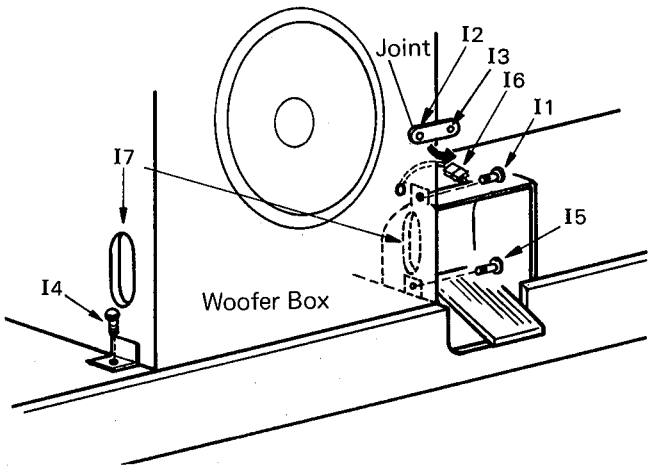


(fig. 16)

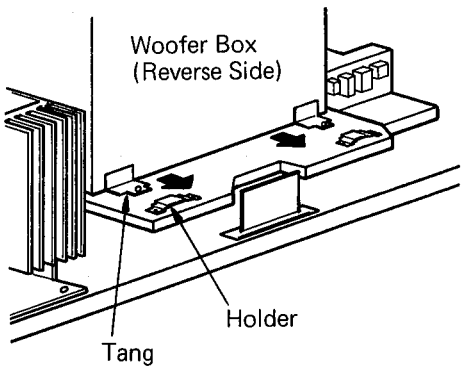
Woofer Box Removal

1) Remove the screw (I1) which fixes the expression cover.
2) Remove the joint retaining screw (I2), loosen the screw (I3), and slide the joint in the direction indicated by arrow.
3) Remove the screw (I4) at the left angle.
4) Remove the screw (I5) at the stand A.
5) Remove the speaker wire harness connector (I6).
6) Put your hands to the handling holes (I7) and draw out the woofer box.

Note on Installation: When installing, insert the woofer box tangs into the holder on the floor board. (fig. 18)



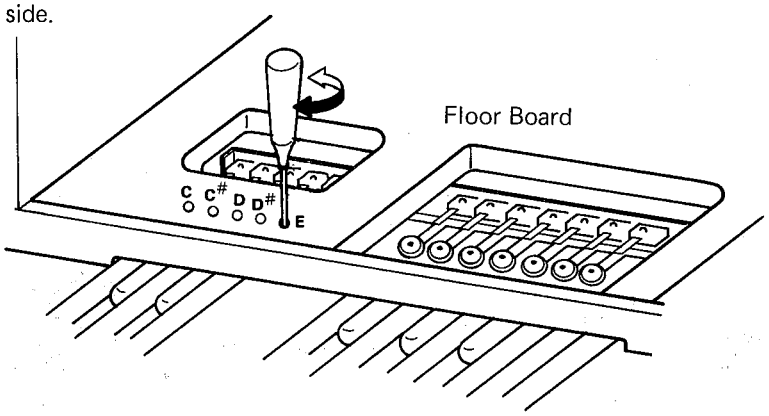
(fig. 17)



(fig. 18)

Pedal Key Retaining Screw Tightening

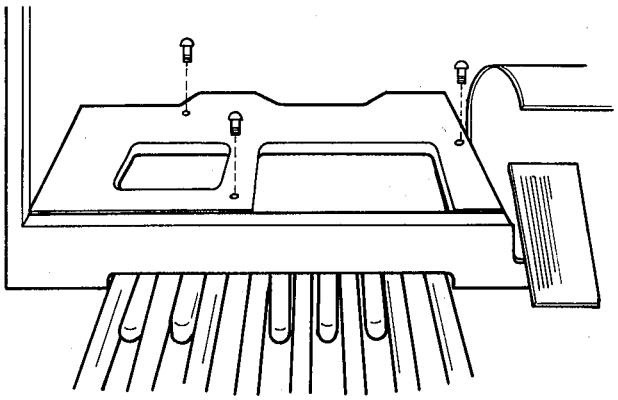
1) Remove the dust cover.
2) The pedal key retaining screw can be tightened by inserting a screwdriver into the holes of the floor board.
3) In the cases of C and C#, remove the PU unit after removing the two retaining screws on the front side and the four connectors on the back side.



(fig. 19)

Floor Board Removal

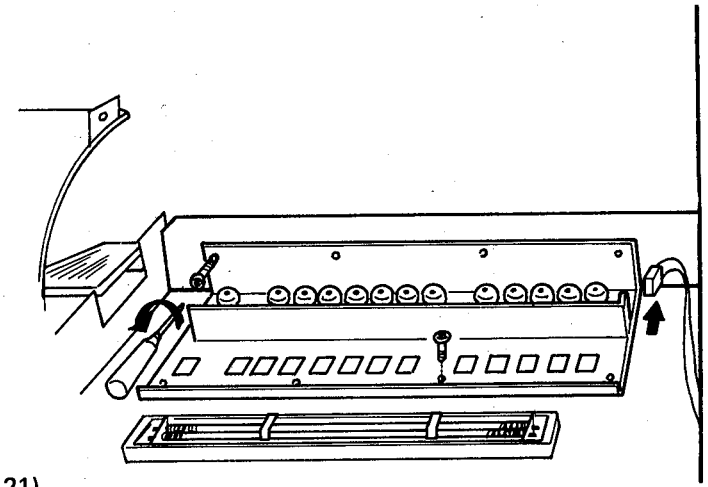
Remove the three retaining screws and take off the floor board.



(fig. 20)

Pedal Keyboard Removal

1) Remove the screws securing the back board.
2) Remove the flat cable connector from the PK.
3) Remove the eight retaining screws securing the PK.
4) Incline the Electone organ toward the rear and pull the PK out.



(fig. 21)

(Reverse Side)

LSI DATA TABLE

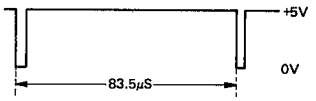
YM2114 SCI (System Controller Interface)

Pin No.	Name	I/O	Function
1	Vss	–	Ground
2	D0	I/O	Data bus
3	D1	I/O	
4	D2	I/O	
5	D3	I/O	
6	D4	I/O	
7	D5	I/O	
8	D6	I/O	
9	D7	I/O	
10	KD1	I	Break contact (block data in)
11	KD2	I	Make contact (block data in)
12	SHE	O	Key multiplex data shift enable (*1)
13	NSi	O	Driving pulse for multiplex note production data.
14	LDE	O	Latch data enable (*3) (*2)
15	iTDAT	O	Initial touch data
16	CR0	O	Key code data 0
17	Vss	–	Ground
18	CR1	O	Key code data 1
19	CR2	O	" 2
20	CR3	O	" 3
21	CR4	O	" 4
22	EGTRA	I	Truncate pulse (← OPA)
23	EGTRB	I	" (← OPB)
24	EGTRE1	I	" (← OPE1)
25	EGTRE2	I	" (← OPE2)
26	LV1	O	Level data 1
27	LV2	O	Level data 2
28	SYNCW	O	Synchro pulse
29	AGND	–	Analog ground
30	AVV	–	Analog DC Supply
31	COMPAD	O	After touch voltage (D/A Converter Out)
32	COMP	I	After touch voltage
33	COMPS	O	After touch voltage for UK, LK, SK
34	L	I	LK after touch voltage in
35	U	I	UK after touch voltage in
36	S	I	SK after touch voltage in
37	EXP	I	EXP voltage in
38	Vss	–	Ground
39	CiD	O	Rhythm sound data (→ OPCW)
40	TEST2	I	Test pin 2
41	PNCC1	O	Panel data controlling data
42	PNCC0	O	"
43	PNCCD	O	Panel event data
44	TDi	I	Preset board (loop data in)
45	SC0	O	Panel loop control data 0
46	SC1	O	" 1
47	TAC0	O	Control data of Preset loop data 0
48	TAC1	O	" 1
49	TB	O	Driving pulse for making Preset board SW scanning
50	SDi	I	Panel loop (serial data in)
51	SDO	O	Panel loop (data out)
52	TEST1	I	Test pin
53	INT1	O	Interrupt data (→ SC)
54	AD0	I	Address buses
55	AD1	I	
56	AD2	I	
57	AD3	I	
58	AD4	I	
59	CE	I	Chip enable (← SCD) (*4)
60	φ2M	I	System control clock φ2M (← SC) (*5)
61	WR	I	Read and Write control
62	+5D	–	Dc supply
63	φ1	I	Master clock pulse (*6)
64	φ2	I	

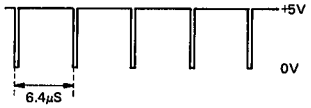
WAVEFORM

*1 SHE (Key OFF)

*2 NSi (Key OFF)

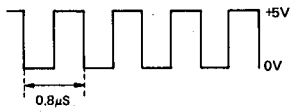


*3 LDE (Key OFF)

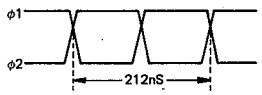


*4 CE

*5 φ2M



*6 φ1, φ2



2ª Placa

YM2025 SC (System Controller)

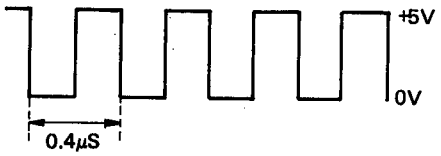
Pin No.	Name	I/O	Function
1	Vss	–	Ground
2	$\overline{WAIT}$	I	Ready data (← SCD) (*1)
3	$\phi 1$	O	System clock 1 (Not used)
4	$\overline{INT1}$	I	Interrupt 1
5	N.C	–	–
6	$\overline{INT0}$	I	Interrupt 2 (Non maskable)
7	SY	–	Not used
8	VDD	–	DC supply
9	AD0	O	Address buses (AD0 ~ AD11)
10	AD1	O	
11	AD2	O	
12	AD3	O	
13	AD4	O	
14	AD5	O	
15	AD6	O	
16	AD7	O	
17	AD8	O	
18	AD9	O	
19	AD10	O	
20	AD11	O	
21	Vss	–	Ground
22	AD12	O	Address buses (AD12 ~ AD15)
23	AD13	O	
24	AD14	O	
25	AD15	O	
26	D7	I/O	Data buses
27	D6	I/O	
28	D5	I/O	
29	D4	I/O	
30	D3	I/O	
31	D2	I/O	
32	D1	I/O	
33	D0	I/O	
34	$\overline{WR}$	O	Read and Write control
35	N.C	–	–
36	N.C	–	–
37	ϕM	I	System clock ϕM (*2)
38	SV	–	+5V
39	$\phi 2$	O	System clock $\phi 2$ (*3)
40	$\overline{IC}$	I	Initial clear (*4)

WAVEFORM

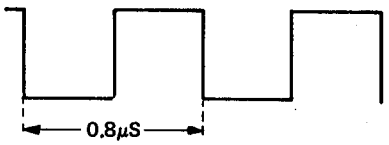
***1 $\overline{WAIT}$**

When the External Memory access is late the $\overline{WAIT}$ terminal voltage became low and the excution of the programmed Fetch cycle.

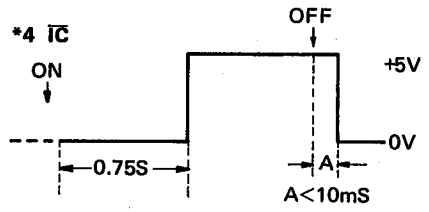
***2 ϕM**



***3 $\phi 2$**



***4 $\overline{IC}$**

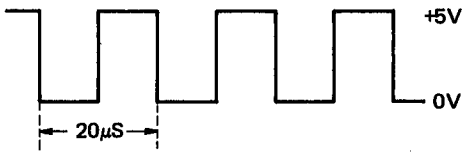


YM2127 TE (Touch Envelope)

Pin No.	Name	I/O	Function
1	CR0	I	Key code data 0
2	iTD	I	Initial touch data
3	$\overline{TEST}$	I	Test pin
4	N.C	–	–
5	N.C	–	–
6	CR0O	O	After touch envelope data
7	SYW	I	Synchro pulse (*1)
8	Vss	–	Ground
9	$\phi 2$	I	Master clock pulse
10	$\phi 1$	I	
11	+5D	–	DC supply
12	N.C	–	–
13	N.C	–	–
14	CR4	I	Key code data 4
15	CR2	I	" 2
16	CR1	I	" 1

WAVEFORM

***1 SYW**

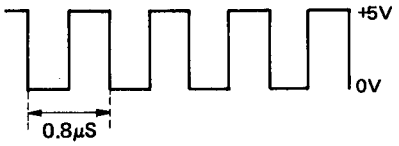


YM5203 SCD (System Control Decoder)

Pin No.	Name	I/O	Function
1	Vss	–	Ground
2	$\overline{\phi 2M}$	I	System clock $\overline{\phi 2M}$ (←SC) (*1)
3	$\overline{WR}$	I	Read and Write control (←SC)
4	$\overline{WAIT}$	O	Ready (*2)
5	$\overline{EIO}$	O	External I/O control
6	AD0	I	Address buses (AD0 ~ AD8)
7	AD1	I	
8	AD2	I	
9	AD3	I	
10	AD4	I	
11	AD5	I	
12	AD6	I	
13	AD7	I	
14	AD8	I	
15	+2D	–	DC Supply (+2V)
16	+5D	–	DC Supply (+5V)
17	Vss	–	Ground
18	AD9	I	Address buses (AD9 ~ AD15)
19	AD10	I	
20	AD11	I	
22	AD12	I	
22	AD13	I	
23	AD14	I	
24	AD15	I	
25	D0	I/O	Data buses
26	D1	I/O	
27	D2	I/O	
28	D3	I/O	
29	D4	I/O	
30	D5	I/O	
31	D6	I/O	
32	D7	I/O	
33	$\overline{CE}$	O	Chip enable (→SC1) (*3)
34	$\overline{MDC}$	O	Electone model code read enable (*4)
35	$\overline{RAM11}$	O	RAM1 output enable
36	$\overline{RAM12}$	O	RAM1 chip enable
37	$\overline{RAM21}$	O	RAM2 output enable
38	$\overline{RAM22}$	O	RAM2 chip enable
39	$\overline{RAM31}$	O	RAM3 output enable
40	$\overline{RAM32}$	O	RAM3 chip enable
41	$\overline{RAM41}$	O	RAM4 output enable
42	$\overline{RAM42}$	O	RAM4 chip enable
43	$\overline{ROM1}$	O	ROM1 chip enable
44	$\overline{ROM2}$	O	ROM2 chip enable
45	$\overline{ROM3}$	O	ROM3 chip enable
46	$\overline{BSEL}$	O	Bank selection
47	$\overline{EMEM}$	O	External memory enable
48	Vss	–	Ground
49	$\overline{ECE2}$	O	E-RAM chip enable
50	$\overline{ECE1}$	O	"
51	ERAM R/W	O	E-RAM (Read and Write) control
52	ECLR	O	E-RAM (address counter) clear data
53	$\overline{ECK}$	O	Clock pulse for making E-RAM address data (*5)
54	ED7	I/O	E-RAM data buses
55	ED6	I/O	
56	ED5	I/O	
57	ED4	I/O	
58	ED3	I/O	
59	ED2	I/O	
60	ED1	I/O	
61	ED0	I/O	
62	VCC	–	DC Supply (+5V)
63	DME	O	Digital Mute Control
64	$\overline{IC}$	I	Initial Clear (*6)

WAVEFORM

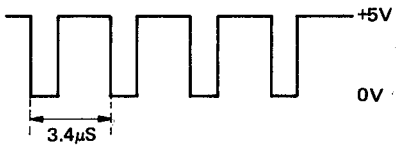
*1 ϕ2M



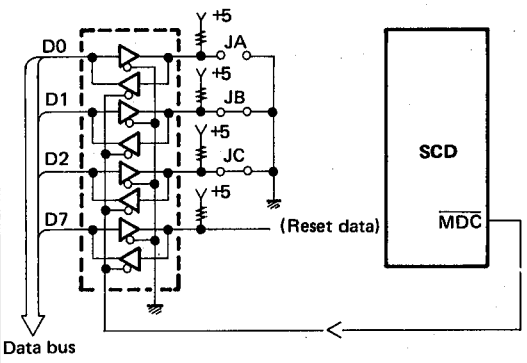
*2 $\overline{WAIT}$

When the External Memory access is late the $\overline{WAIT}$ terminal voltage became low and the excution of the programmed Fetch cycle.

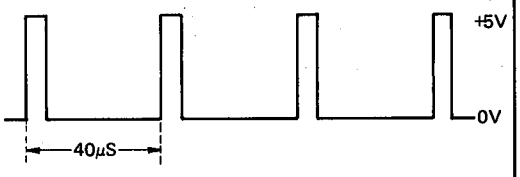
*3 $\overline{CE}$



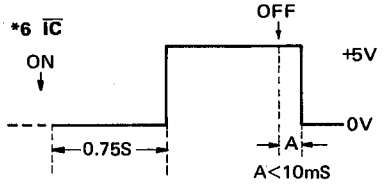
*4 $\overline{MDC}$



*5 $\overline{ECK}$ (CONFIRM & WRITE SW ON)



*6 $\overline{IC}$



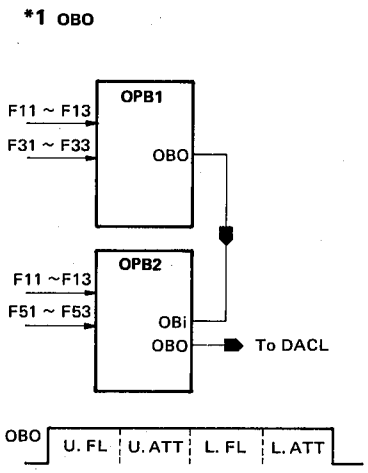
YM2115 PG (Phase Generator)

Pin No.	Name	I/O	Function	WAVEFORM
1	Vss	—	Ground	
2	TX1	I	Test pin	
3	TX2	I		
4	TX3	I		
5	TX4	I		
6	$\overline{Ti}$	I		
7	$\overline{IC}$	—	Initial Clear	
8	PNCD		Panel data	
9	$\overline{LED3}$	I	Panel data (load enable)	
10	CR0	I	Key code data 0	
11	N.C	—	—	
12	N.C	—	—	
13	N.C	—	—	
14	N.C	—	—	
15	CR4	I	Key code data 4	
16	CR3	I	" 3	
17	SYW	I	Synchro pulse	
18	CR2	I	Key code data 2	
19	CR1	I	" 1	
20	N.C	—	—	
21	N.C	—	—	
22	$\overline{IC}$	I	Initial Clear	
23	E	I	Output enable	
24	F14	O	Phase data for primary note	
25	F13	O		
26	F12	O		
27	F11	O		
28	N.C	—	—	
29	F33	O	Phase data for 3rd note	
30	F32	O		
31	F31	O		
32	N.C	—	—	
33	F53	O	Phase data for 5th note	
34	F52	O		
35	F51	O		
36	N.C	—	—	
37	FV3	O	Phase data for vibrato	
38	FV2	O		
39	FV1	O		
40	N.C	—	—	
41	FE3	O	Phase data for OPE	
42	FE2	O		
43	FE1	O		
44	N.C	—	—	
45	N.C	—	—	
46	VDD	—	DC Supply	
47	$\phi 1$	I	Master clock pulse	
48	$\phi 2$	I		

YM2117 OPB (Operator-B)

Pin No.	Name	I/O	Function
1	Vss	—	Ground
2	TRB	O	Decay data for truncate
3	N.C	—	—
4	N.C	—	—
5	CRϕ0	I	After touch envelope data
6	LV2	I	Amplitude level data 2
7	—		
8	OBi	I	Tone signal data from other OPB
9	OBO	O	Tone signal data (*1)
10	F13	I	Phase data for primary note
11	F12		
12	F11	I	
13	F33	I	Phase data for 3rd note
14	F32	I	
15	F31	I	
16	CR1	I	Key code data 1
17	CR2	I	" 2
18	LED	I	Panel data (load enable)
19	PNCD	I	Panel data
20	N.C	—	—
21	SYW	I	Synchro pulse
22	+5D	—	DC supply
23	ϕ1	I	Master clock pulse
24	ϕ2	I	

WAVEFORM



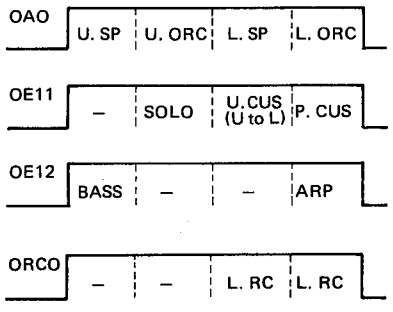
YM806 OPA (OPE·OPRC) (Operator)

Pin No.	Name OPA	Name OPE	Name OPRC	I/O	Function
1	Vss	Vss	Vss	—	Ground
2	SYW	SYW	SYW	I	Synchro pulse
3	ϕ1	ϕ1	ϕ1	I	Master clock pulse
4	ϕ2	ϕ2	ϕ2	I	
5	Vss	Vss	Vss	—	Ground
6	TRA	TR	TRRC	O	Decay data for truncation
7	LV1	LV2	LV1	I	Amplitude level data
8	iTD	iTD	iTD	I	Initial touch data
9	CR2	CR4	CR2	I	Key code data
10	CR00	CR00	CR00	I	"
11	CR1	CR3	CR1	I	"
12	PNCD	PNCD	PNCD	I	Panel data
13	LED	LED	LED	I	Panel data (load enable)
14	F14	N.C	N.C	I	
15	F13	E3	F13	I	Phase data
16	F12	E2	F12	I	
17	F11	E1	F11	I	
18	V3	N.C	N.C	I	Phase data for vibrato
19	V2	N.C	N.C	I	
20	V1	N.C	N.C	I	
21	+5D1	+5D1	+5D1	—	
22	+5D2	+5D2	+5D2	—	
23	N.C	OE12	N.C	O	Tone signal data
24	OAO	OE11	ORCO	O	" (*1)

WAVEFORM

YM806IC functions as OPE or OPRC based on PNCD data.

*1 OAO · OE · ORCO Output timing

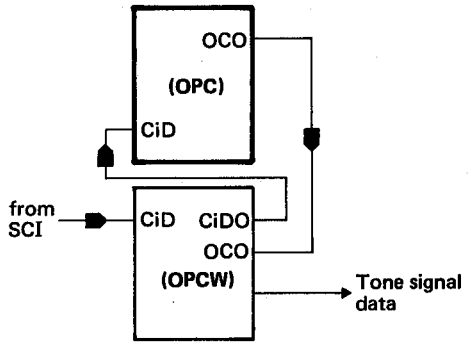


YM2118 OPC (Operator-C)

Pin No.	Name	I/O	Function
1	Vss	—	Ground
2	CR0	I	Key code data 0
3	TEST-E	I	Test pin
4	TO1	I	"
5	TO2	I	"
6	TO3	I	"
7	TEST-D	I	"
8	TO4	I	"
9	OC0	O	Tone signal data (*1)
10	TEST	I	Test pin
11	TEST-ABC	I	"
12	LV2	I	Amplitude level data 2
13	SYW	I	Synchro pulse in
14	N.C	—	—
15	N.C	—	—
16	N.C	—	—
17	N.C	—	—
18	N.C	—	—
19	CiD	I	Rhythm sounds data (*1)
20	LED	I	Panel data load enable
21	PNCD	I	Panel data
22	φ2	I	Master clock pulse
23	φ1	I	Master clock pulse
24	+5D	—	DC supply

WAVEFORM

***1 CiD · OCO terminal connections**

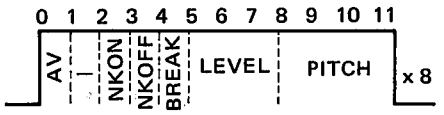


YM2124 OPCW (Operator-CW)

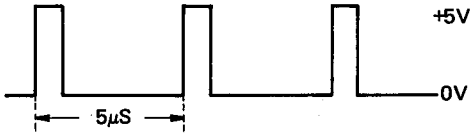
Pin No.	Name	I/O	Function
1	Vss	–	Ground
2	OC0	I	Tone signal data from OPC
3	CiD	I	Rhythm sounding data (*1)
4	LV2	I	Amplitude level data 2
5	PNCD	I	Panel data
6	LED6	I	Panel data load enable
7	WD0	I	Data
8	WD1	I	
9	WD2	I	
10	WD3	I	
11	WD4	I	
12	WD5	I	
13	WD6	I	
14	WD7	I	
15	WA0	O	Address
16	WA1	O	
17	WA2	O	
18	WA3	O	
19	WA4	O	
20	WA5	O	
21	WA6	O	
22	WA7	O	
23	WA8	O	
24	WA9	O	
25	WA10	O	
26	WA11	O	
27	WA12	O	
28	WA13	O	
29	WA14	O	
30	WA15	O	
31	WA16	O	
32	WA17	O	
33	$\overline{CE}$	I	Chip enable (*2)
34	CR0	I	Key code data
35	SYW	I	Synchro pulse
36	OCWO	O	Tone signal data (*3)
37	CiDO	O	Rhythm sounding data to OPC
38	+5D	–	DC supply
39	ϕ1	I	Master clock pulse
40	ϕ2	I	

WAVEFORM

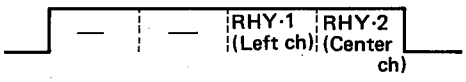
***1 CiD**



***2 CE**



***3 OCWO Out put timing**



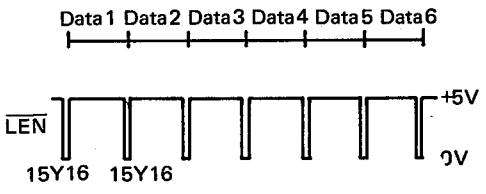
YM2119-1. 2. 3 DGF (Degital Filter)

Pin No.	Name	I/O	Function	WAVEFORM
1	Vss	—	Ground	
2	I1	I	Tone signal data from OP	
3	I2	I		
4	I3	I		
5	$\overline{LED}$	I	Panel Data load enable	
6	PNCD	I	Panel Data	
7	SYW	I	Synchro pulse	
8	Qi	I	Synchro pulse for filter coefficient data (not used)	
9	$\overline{QX}$	O	"	
10	$\overline{KX}$	O	Check data of filter coefficient data (not used)	
11	$\overline{Fi}$	I	Filter compensation data (from before stage filter)	
12	$\overline{BX}$	O	Filter compensating data (feed back) for before stage filter	
13	$\overline{IC}$	I	Initial clear	
14	$\overline{Bi}$	I	Filter compensation data (feed back) from next stage filter	
15	$\overline{FX}$	O	Filter compensation data to next stage filter	
16	$\overline{KS}$	I	Switching data of $\overline{Ki}$ filter coefficients and internal tones (not used)	
17	$\overline{Ki}$	I	External filter coefficients data (not used)	
18	E	I	Output enable (not used)	
19	O3	O	Tone signal (filtered)	
20	O2	O		
21	O1	O		
22	+5D	—	DC supply	
23	ϕ1	I	Master clock pulse	
24	ϕ2	I		

YM2120 DACL (DAC Logic)

Pin No.	Name	I/O	Function	WAVEFORM
1	Vss	—	Ground	
2	OAO1	I	Tone signal data from DGF	
3	OAO2	I		
4	OAO3	I		
5	OBO	I	Tone signal data from DGF	
6	OEO11	I	Tone signal data from DGF	
7	OEO21	I		
8	OEO12	I	Tone signal data from OPE	
9	OEO22	I		
10	PNCD	I	Panel data	
11	LED5	I	Panel data load enable	
12	ORCO	I	Rhythmic chord signal data	
13	OCWO	I	Rhythm signal data	
14	$\overline{LEN}$	O	Load enable	
15	SHEN	O	Sample and hold enable	
16	REVO	I	Reverb signal data	
17	DACO1	O	Tone signal data 1 (*1)	
18	DACO2	O	Tone signal data 2	
19	N.C	—	—	
20	SYW	I	Synchro pulse	
21	$\overline{TEST}$	—	Test pin	
22	+5D	—	DC supply (+5V)	
23	ϕ1	I	Master clock pulse	
24	ϕ2	I		

*1 DACO1 · DACO2



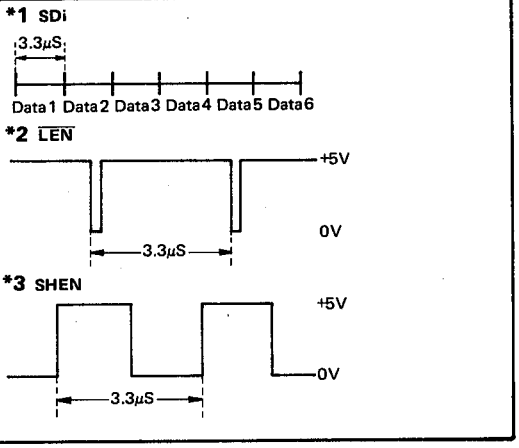
YM1035 SEC III (Symphonic Ensemble Clock Generator III)

Pin No.	Name	I/O	Function	WAVEFORM
1	TC	I	Tremolo speed control	
2	–5V	–	DC supply (–5V)	
3	LC	O	Output signal (level setting voltage)	
4	$\overline{C}$	I	Chorus ON (data in)	
5	$\overline{T}$	I	Tremolo ON (data in)	
6	LFN	I	FN1·FN2 output signal setting voltage	
7	LFW	I	FW1·FW2 "	
8	Vss	–	Ground (0V)	
9	FW1	O	Clock pulse control signal TR-4.8 ~ 7.2Hz CH-1.2Hz	
10	FW2	O	" TR-4.8 ~ 7.2Hz CH-1.2Hz	
11	FN1	O	" TR-9.6 ~ 14.4Hz CH-0.6Hz	
12	FN2	O	" TR-9.6 ~ 14.4Hz CH-0.6HZ	
13	VDD	–	DC supply (–9V)	
14	TTC	I	Transition time control data (Tremolo ⟷ Chorus)	
15	TRC	I	C.R for oscillator	
16	TA	I	Tremolo speed adjustment	

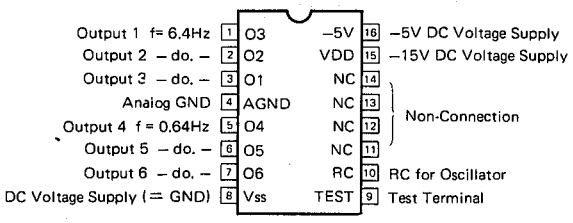
4a Placa

iG06500 DAC (Degital to Anlog Conveter)

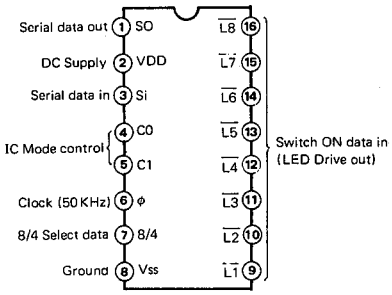
Pin No.	Name	I/O	Function	WAVEFORM
1	O.SADJ	I	Off set voltage (adjustment)	*1 SDi
2	VREF	I	DC 2.1V reference voltage	
3	VDD(+5D)	–	DC supply (+5V)	
4	SDi	I	Tone signal data (*1)	
5	$\overline{LEN}$	I	Latch load enable (*2)	
6	DG	I	Digital GND	
7	ϕD	I	Clock pulse (4.8 MHz)	
8	SHEN	I	Sample and hold enable (*3)	
9	CH0	O	Analog converted tone signal	
10	CH1	O		
11	CH2	O		
12	CH3	O		
13	CH4	O		
14	CH5	O		
15	VEE	–	Analog DC supply (–12V)	
16	Vcc	–	Analog DC supply (+12V)	
17	TP	–	Test pin	
18	EA	I	Analog GND	



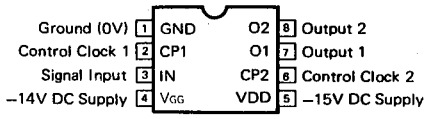
• YM60800
String Ensemble Clock Generator



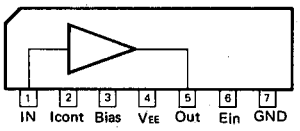
• YM21210
DRV



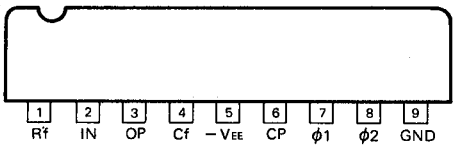
• YM35100
Low Noise 512 Stage BBD



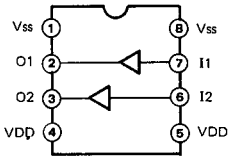
• iG02600
Voltage Controlled Amplifier



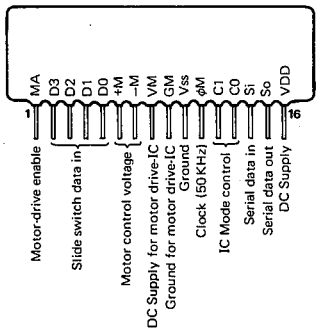
• iG03290
BBD Clock Driver



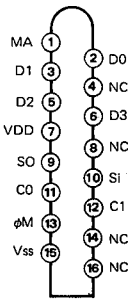
• iG07950
Clock Buffer



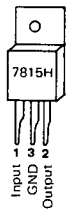
• iG 06450
DRM1



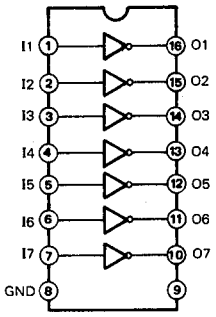
• iG07110 (DRM2)



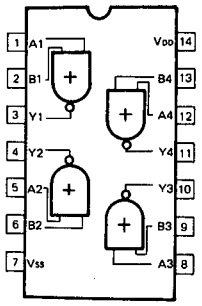
● **μPC7815H** (iG 063900)
3 terminals Regulator [Vo = +15V]



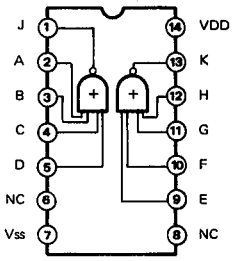
● **TD62103P** (iG67700)
Transistor Array



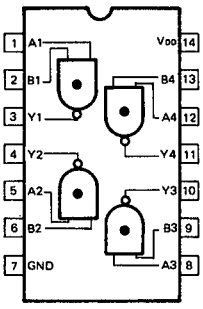
● **TC4001BP** (iG 001170)
NOR Gate



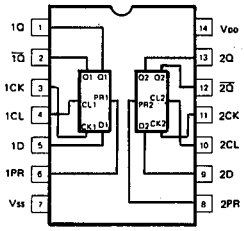
● **TC4002BP** (iG09680)
Dual 4-Input NOR Gate



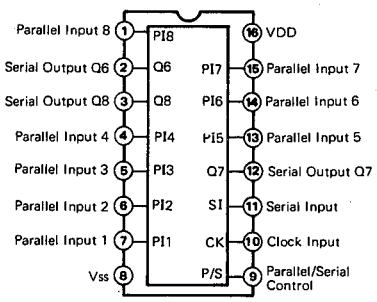
● **TC4011BP** (iG001240)
Quad 2 – Input NAND Gate



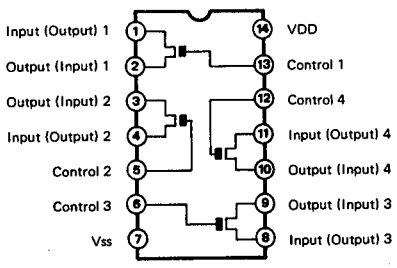
● **TC4013BP** (iG001180)
Dual D – Type Flip-Flop



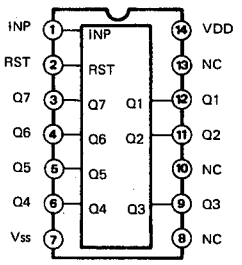
● **TC4014BP** (iG 094200)
8-Stage Synchronous Shift Register with Parallel or Serial Input / Serial Output



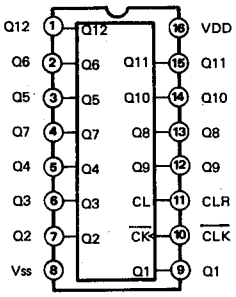
● **TC4016BP** (iG001690)
Quad Bilateral Switch



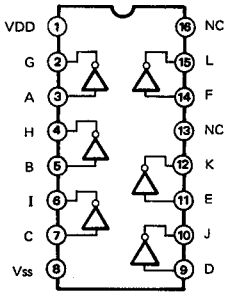
● **TC4024BP** (iG03810)
7-Stage Binary Ripple Counter



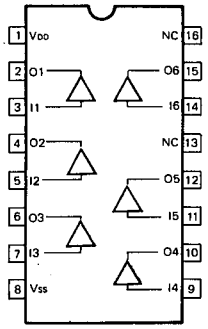
● **TC4040BP** (iG05240)
12-Stage Binary Ripple Counter



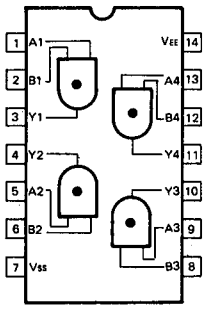
● **TC4049BP** (iG00126)
Hex Buffer/Converter (Inverting)



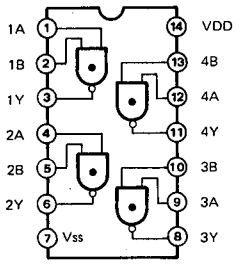
● **TC4050BP** (iG001740)
Hex Buffer/Converter
Non-Inverting Type



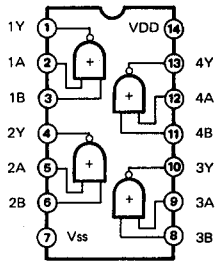
● **TC4081BP** (iG001760)
Quad 2 – Input AND Gate



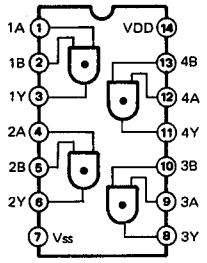
● **HD74S00** (iG02690)
● **HD74LS37** (iG05340)
● **TC40H000P** (iG08070)
Quad 2-Input NAND Buffers



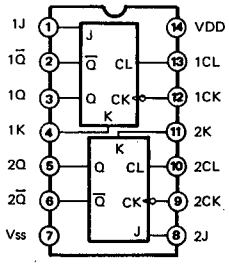
● **TC40H002P** (iG09630)
Quad 2-Input NOR Gate



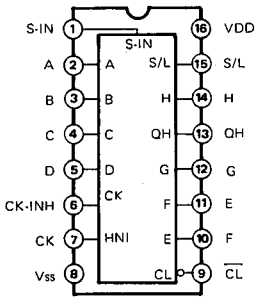
● **TC40H008P** (iG09640)
Quad 2-Input AND Gate



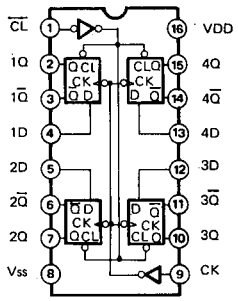
● **TC40H107AP** (iG09650)
Dual J-K Master-Stave F/F



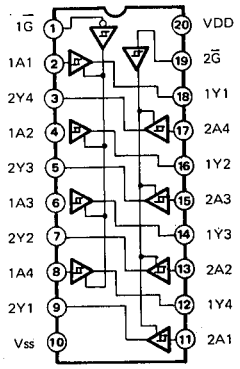
● **TC40H166P** (iG09660)
8-bit Shift Registers



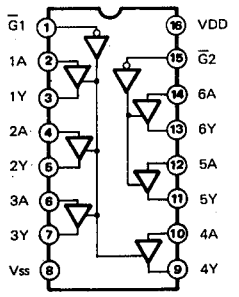
- **TC40H175P** (iG09670)
  Quad D-Type F/F



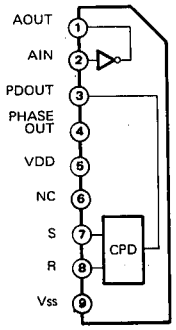
- **HD74LS241** (iG09690),
- **TC40H244P** (iG10720)
  Octal 3 State Bus Buffers



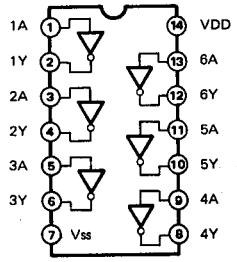
- **HD74LS367** (iG05040),
- **TC40H367P** (iG10730)
  Hex 3 State Bus Buffers



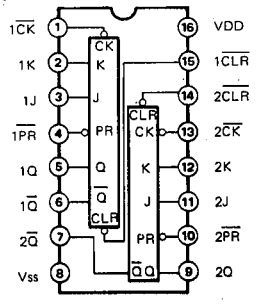
- **TC5081P** (iG079400)
  Phase Comparator



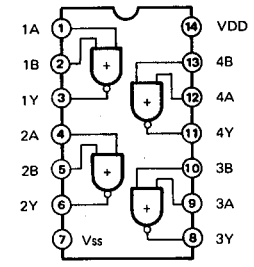
- **HD74S04** (iG05870)
- **HD74LS04** (iG02701)
  Hex Inverters



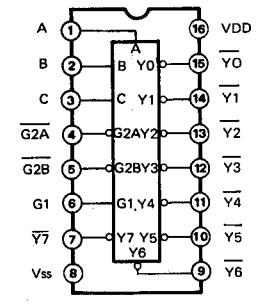
- **HD74LS112** (iG07930)
  Dual JK F/F with Preset and Clear



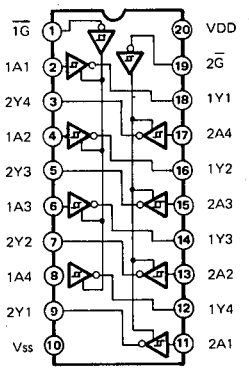
- **HD74LS02** (iG02900)
  Quad 2-Input NOR



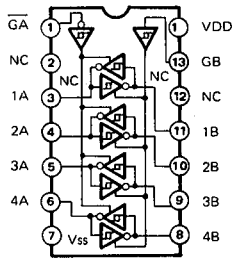
- **HD74LS138** (iG04420)
  3 to 8 Demultiplexer



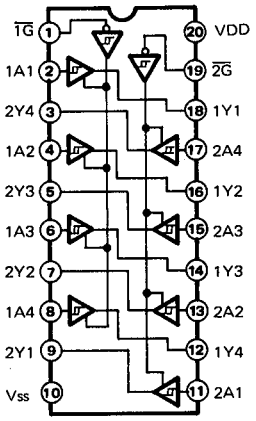
- **HD74LS240** (iG04450)
  Octal 3 State Bus Inverters



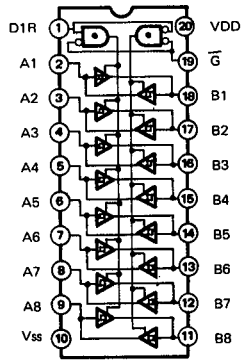
● **HD74LS243** (iG09700)
Quad 3 State Bus Transceivers



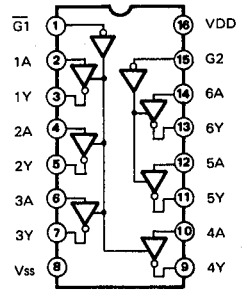
● **HD74LS244** (iG06000)
Octal 3-state Bus Buffers



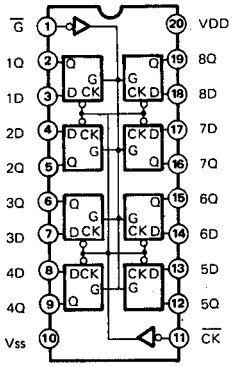
● **HD74LS245** (iG06010)
Quad 3 State Bus Transceivers



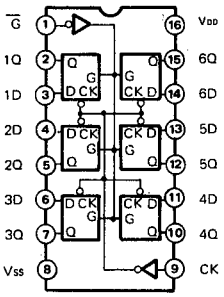
● **HD74LS368A** (iG05050)
Hex 3 State Bus Inverters



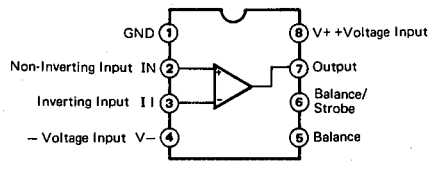
● **SN74LS377** (iG09720)
8 bit D-F/F



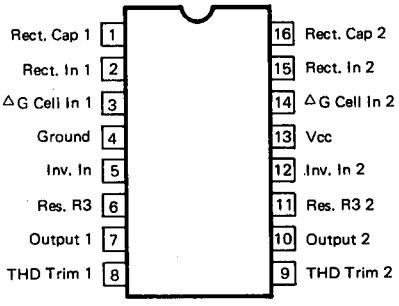
● **SN74LS378** (iG07920)
6 bit D-F/F



● **μPC311** (iG 033400)
Voltage Comparator



● **NE570N** (iG031300)
Compandor



● **NJM4558** (iG00139)
Dual Operational Amplifier